Method and apparatus for generating a pipelined synchronized circuit representation of a program loop. A dependence graph is generated from the program loop. The dependence graph represents operations and registers and connections therebetween. A minimum clock period and initiation interval are determined from the dependence graph. Until a scheduled graph is successfully generated, repeated attempts are made to generate a scheduled graph from operations and registers of the dependence graph using the minimum clock period and the initiation interval. With each failed attempt to generate a scheduled graph, the minimum clock period is increased prior to the next attempt to generate a scheduled graph.